Four Years Underground at Rustrel: Alpha Upset Rate Story in Flip-Chip FPGA Devices at 130nm

A. Lesea, K. Castellani-Coulié, C. Sudre, D. Boyer

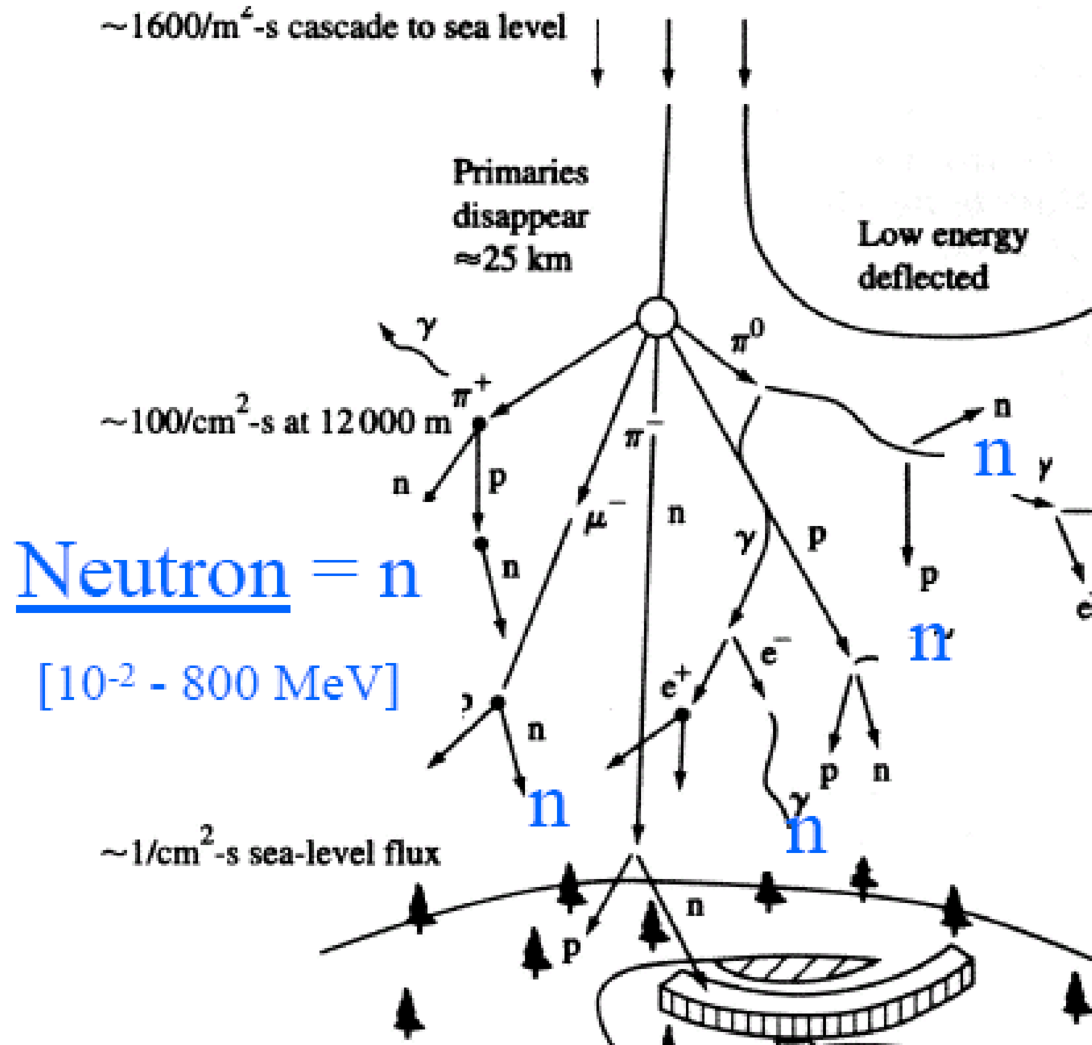
iDUST

June 2010

The Problem

- As geometries shrink to nanometer dimensions in integrated electronic devices, the charge stored diminishes
- Alpha particles are emitted by impurities in the various assembled materials
- These alpha particles easily upset the state of a memory, and also may cause a transient flault (1>0>1)
- Atmospheric neutrons also upset the bits, so we need a place ‘without’ neutrons (…LSBB)

Cosmic Rays
in the earth atmosphere



Objectives

- Is the process of assembly, and the materials used, following the proper process to insure that alpha upsets are below the level required by the product soft error reliability objectives?
- What is the upset rate from alpha particles in the devices?

- Ultra Low Alpha (ULA) Materials used throughout
  - Solder
  - Mold compounds
  - Machinery used is only used with ULA materials
  - Lots of raw materials certified by supplier, and retested by assembly house
  - 'Certificates of compliance' (CoC) on record for every lot assembled with actual cph/cm^2 alpha counts measured

Can the Objectives be Met (Quickly)?

- Once the process is fixed, and suppliers contracted, how long does it take to qualify that everything has been done properly?
  - Experience has shown that the upset rate for using the wrong materials, or having contamination, ranges from a minimum of 6X worse upset rate, to more than 100X worse upset rate
  - Test must supply a reasonable confidence that we are not contaminated, in less than 6 months, by testing a reasonable sample size (100 to 200 parts)
- Can we predict the results before assembly (if done right?)

Five Methods

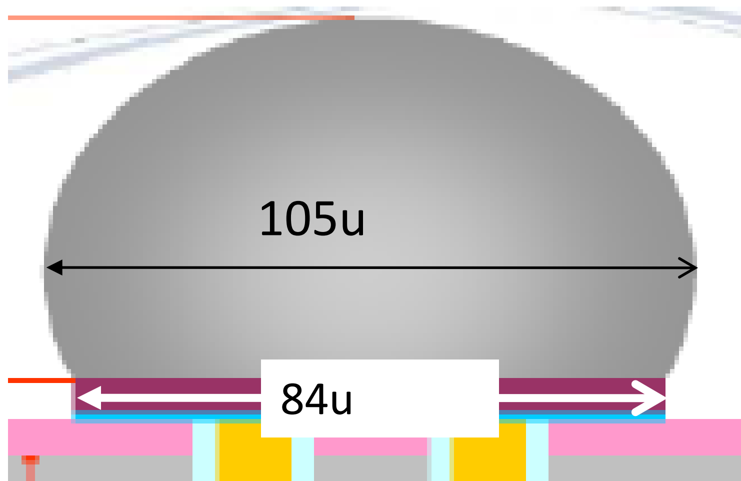
- Rosetta: Two or more altitudes
- LSBB: direct measurement
- Use known contaminated materials(?): overwhelm neutron upsets
- Predict using Thorium foil: JEDEC89A extrapolated
- Predict using simulations

What if We Fail?

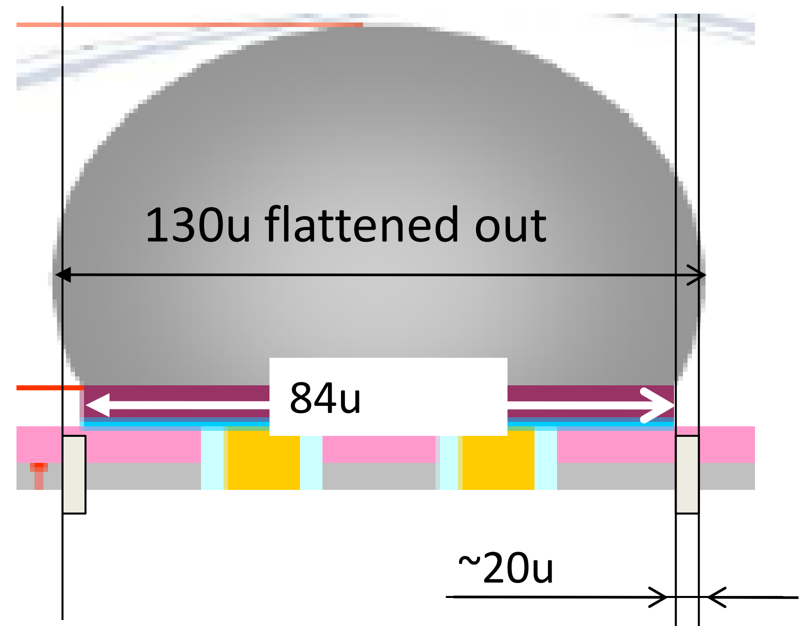
- Contaminated assembly lots cost $10M to contact all customers, discuss the problem, replace
- Xilinx is the only company to publicly admit to a contamination issue, with recall, and file the loss with the SEC

The Problem: C4 Lead Bump

C4 before packaging

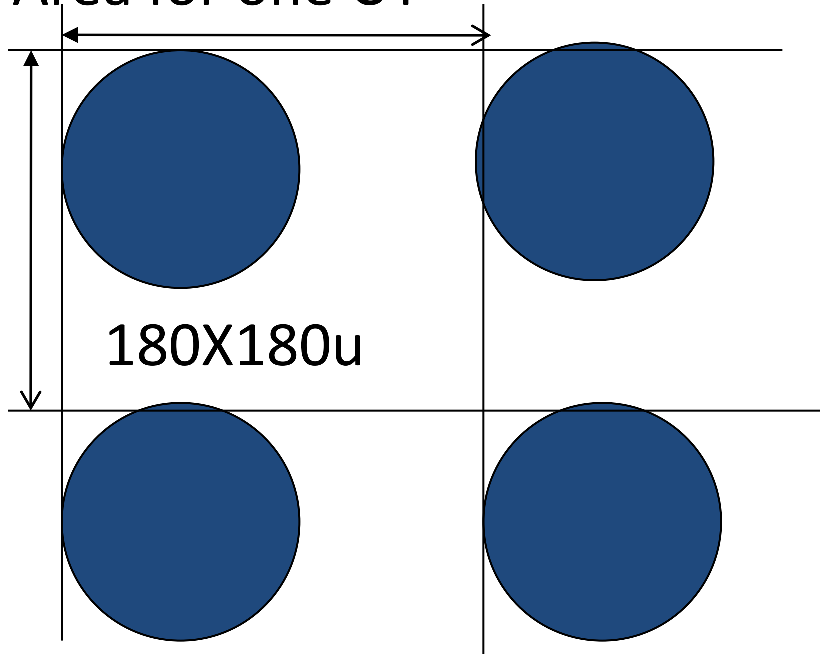


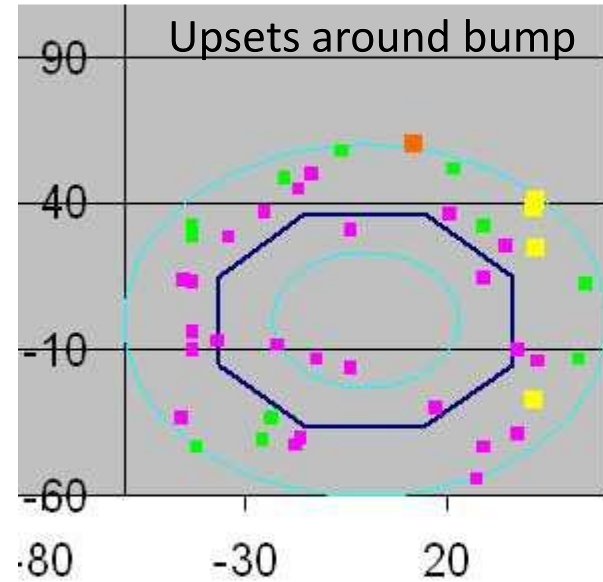
C4 after packaging



Upsets occur around perimeter of the bump in a ‘donut’ shape from the slight overhang, and the density of the metal directly below the bump (via stack) which blocks upsets directly below

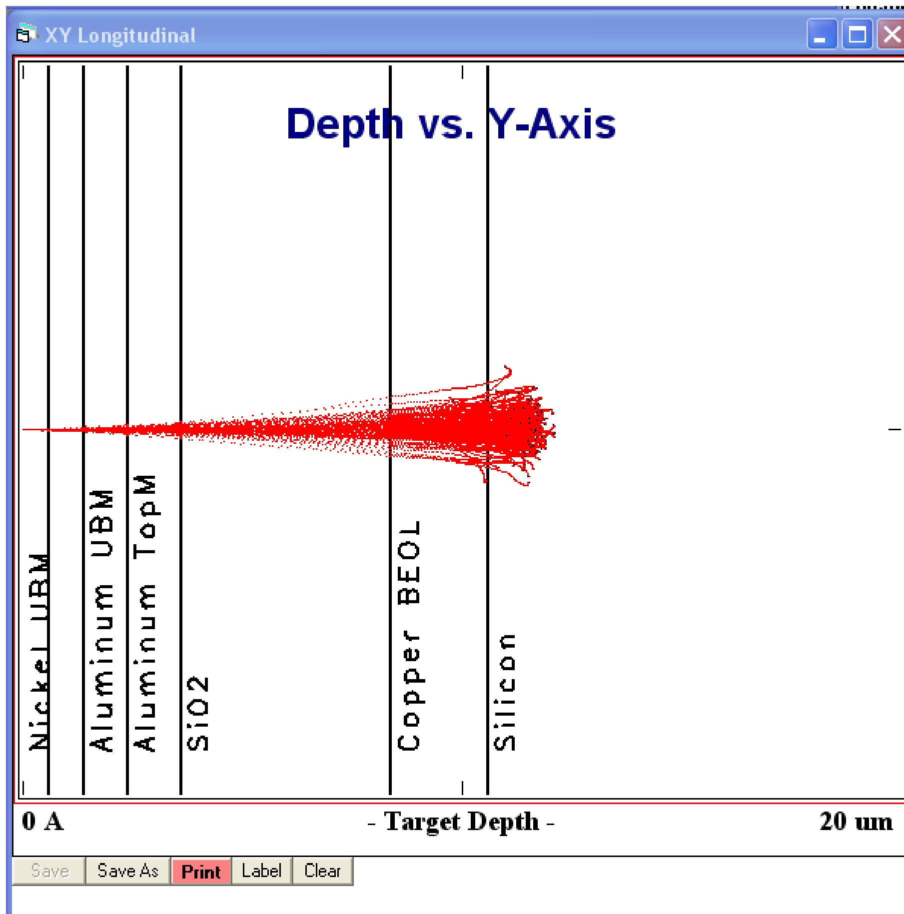
α-SEU: relative estimate C4 bump





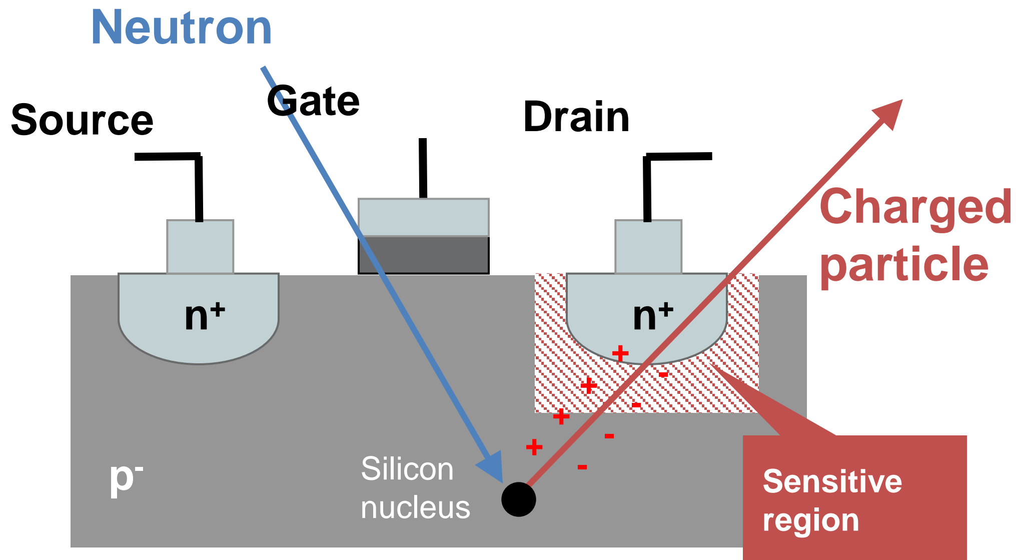
Data from a regular solder lot, built in 2003, which led to the ULA process. From multiple devices in the array. Activity of this material in this lot caused one upset ~ 80 days per device.

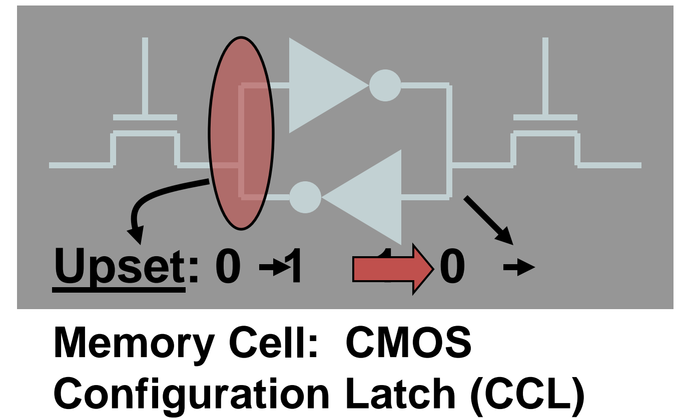
SRIM for alpha particle @ 5 MeV



- Alpha particles penetrate to, and decay in, the active region
- SRIM = Stopping Range In Matter

Soft Errors in CMOS Circuits





Rosetta Experiment

- Arrays of 100 devices
- Controlled by a PC on the Xilinx Intranet
- Data collected every 20 minutes, to every hour on all 100 parts
- At present, 5 arrays of 65nm, 2 arrays of 45 nm at four locations
- Still have 2 arrays of 130nm (at LSBB) collecting data
  - 90nm is officially 'fini' but data collected now is only used for research
- Historically, up to 23 arrays were operating at once
- Detailed in:
  - The Rosetta Experiment: Atmospheric Soft Error Rate Testing in Differing Technology FPGAs, IEEE Transactions on Device and Materials Reliability, Vol. 5, No. 3, September 2005 and subsequent papers

Result of Least Mean Squares Error Best Fit from Rosetta Data

- From the various altitudes of Rosetta arrays we solve for atmospheric and alpha upsets separately for each site using result with the LMSE
  - 70 FIT/Mb, from 37 to 119, for 95% CI for number of events
- Method takes a very long time, with multiple arrays, at multiple altitudes (In this case from 2003 to today)
- Years of data required at “sea level” (Xilinx in San Jose USA, Paul Cézanne Université, Aix-Marseille III, France)
- As well as years of data at higher altitudes (Mauna Kea Hawaii, White Mountain California, Longmont Colorado, Albuquerque New Mexico, Pic du Bure France)
- Subject to inaccuracies in flux prediction at the various latitudes, longitude, and altitude sites

Results from LSBB

- “Quiet” environment: No neutrons > 1 MeV
- The only upsets that occur must be from alpha particles
- 200 devices, 5.86 million device hours
  - 101 FIT/Mb, from 44 to 200 FIT/Mb 95% CI
- “Direct” measurement
- Still few upsets (8)
- Still a very long time to wait if you want the actual upset rate to any degree of confidence

Wrong Solder: Results from a "contaminated lot"

- One lot of Virtex II Pro was assembled with regular solder
- Flux was ~ 4000 cph/cm^2 (ULA material is ~ .005 !!!)
- Devices were actually built into a Rosetta Array
- Physical XY locations of upsets mapped to layout

  – Note: if we intentionally introduce high alpha materials into a ULA facility, we risk contamination. These lots must be assembled elsewhere, and since ULA is now the 'standard' in the Xilinx flow it has become difficult to assemble devices with high alpha solder
  – "Regular solder " varies greatly in cph/cm^2: to do this properly, we would require irradiated solder with known activity levels

Wrong Solder, cont.

- ~14% of die area is 'exposed' to solder bump
- ULA bump is .005 cph/cm2 so flux is .0007 cph/cm2
- Thorium foil also used to cause tens of thousands of upsets on a Virtex II Pro wire bond part to calibrate sensitivity to alpha upsets
- Thorium foil result scaled by the ratio of predicted flux for C4 based on area exposed
  - 82 FIT/Mb (95% CI +/- 3%)
  - Additional errors from actual alpha count of solder bump used, using Thorium to predict decay products in Lead …

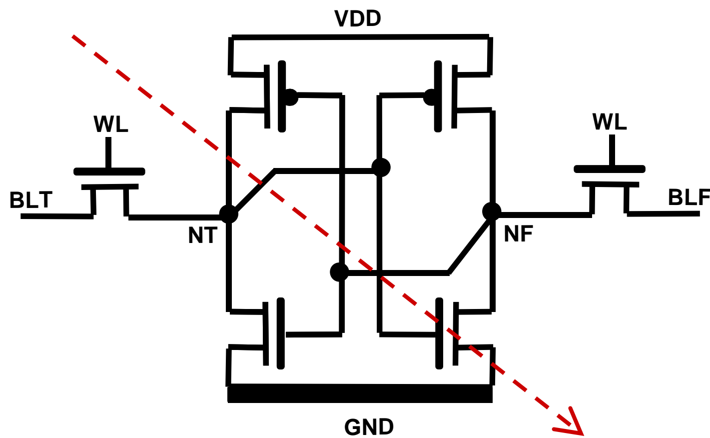
Aside: Contaminated Wire Bond Assembly Result

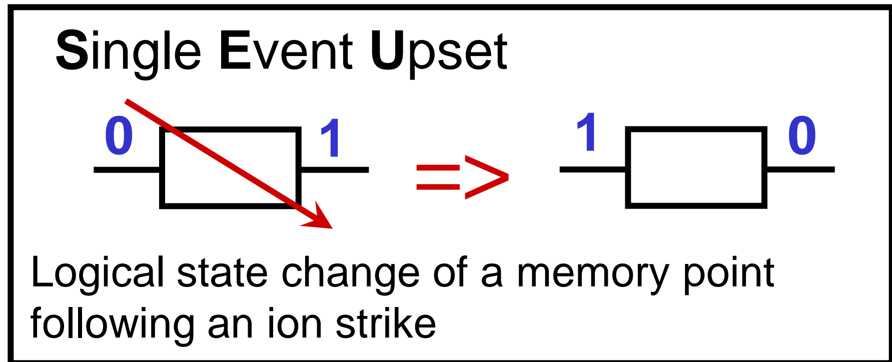
- Wire bond packages are susceptible to contamination
- Lot was assembled with “regular” mold compound
  - Filler in compound was bauxite (raw aluminum ore)
  - Resulted in 6X increase in sea level upset rate
  - Results fell in half every 138 days
  - Contaminant: Polonium 210?
  - Array irradiated at LANSCE for 72 hours while testing other arrays
  - Resulted in re-activating Polonium 210 decay products
  - Upset rate was now >>6X, again with ½ life of ~ 138 days

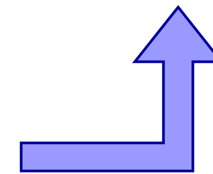
- Polonium 210 present in fertilizer, cigarette smoke, air ionizers…

Predictions from Simulations

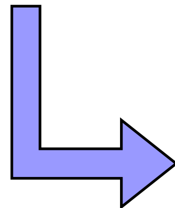
➡ Crossing of an ionizing particle is able to induce a **SEU**

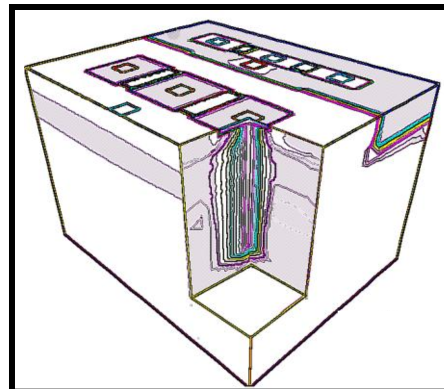






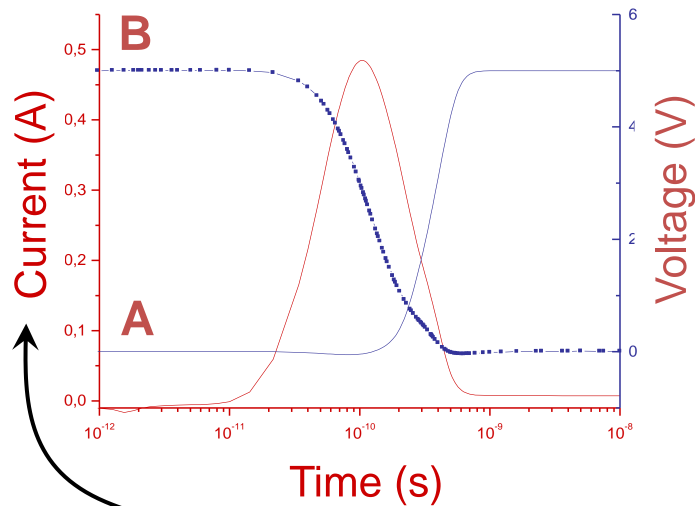
Matter ionization
↳ e⁻-h+ pairs creation





Creation of a parasitic current in the strike through the transistor

Predictions from Simulations



The SEU occurrence will depend on:

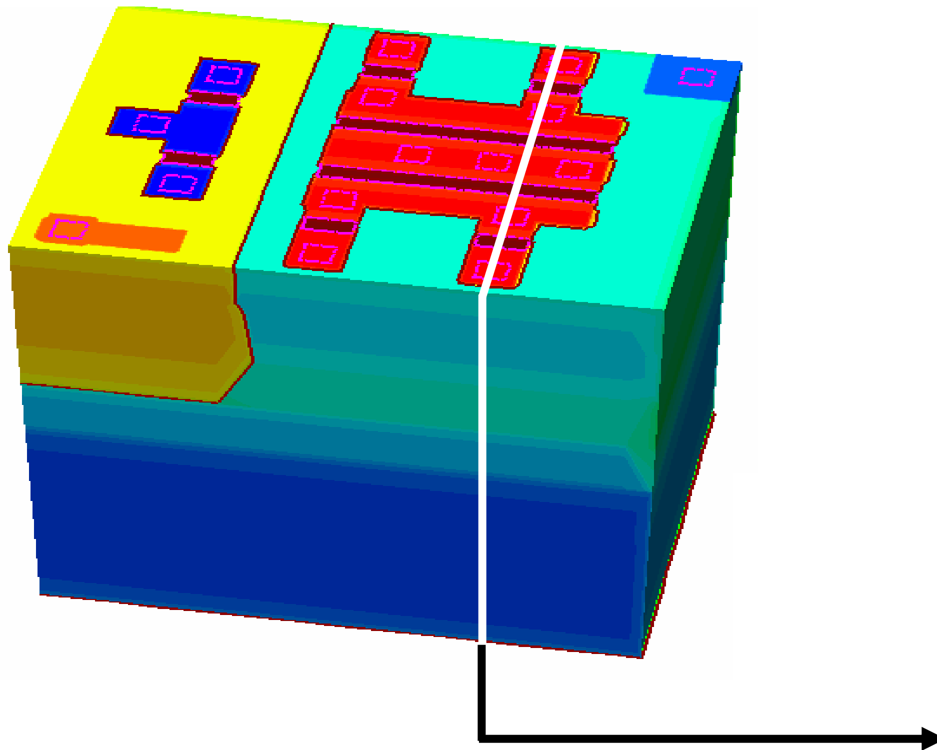
- ✓ **Where** the ion crosses the device
- ✓ Its energy and **LET**
- ✓ The **sensitivity** of the device

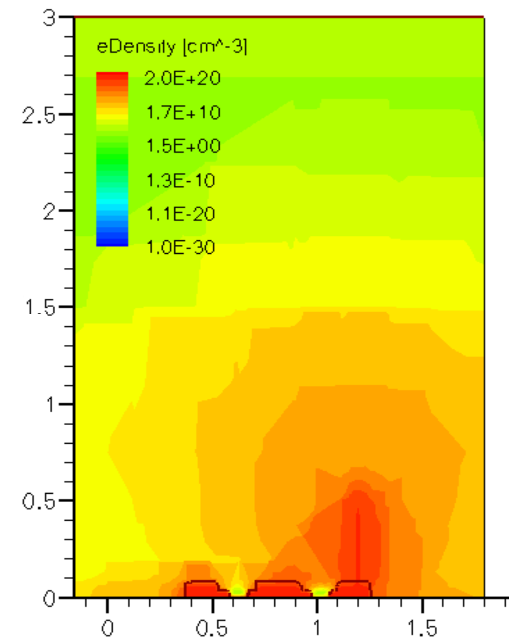
Gate
Drain
Source
Neutron
Ionizing particle

VDD
WL
WL
BLT
BLF
NT
NF
A
B
GND

Predictions from Simulations

Aim of the TCAD simulation work:
Study physical mechanisms within the device in order to extract metrics for SER simulations





After Simulation …

- Develop a database of nuclear interactions for the particle(s) to be studied
  - neutrons, protons, or in this case: alpha particles
  - tracks for each particle, energy deposited
- Run the physical/electrical simulation for all "events" in the database
- Average out the results to provide a ‘cross-section’
  - how many alpha particles, on average, it takes to upset one bit
- Use this ‘cross section’, and the prediction/measurement of the environment to calculate a FIT/Mb rate
  - the solder bump area, die area, and the counts per minute of the ultra-low alpha solder bumps...
- “What number do you wish?” Simulation requires testing to have any confidence in the results

The Numbers (95% CI)

- Rosetta 70 FIT/Mb, from 37 to 119
- LSBB 101 FIT/Mb, from 44 to 200
- JEDEC89A/Th 82 FIT/Mb, from ? to ?
- Predict ??? FIT/Mb, from ? to ?

Five Methods: Summary

- Rosetta
  - Takes many arrays of 100 devices each, at various altitudes
  - Some arrays must spend years at sea level
  - May take more than one year to verify a 6X contamination issue
- LSBB
  - One or two arrays of 100 devices required
    - Lately, even “small” devices have sufficient number of bits to need only one array of 100 components
  - Verification that contamination is not present takes < ½ year
- Use known contaminated materials(?)
  - Dangerous! Who will assemble these? How contaminated? With what?
- Predict using Thorium foil
  - Succession of estimations, no actual measurement of real product
  - Good for estimation, before product is in production status
  - Thorium decay chain is not equal to Actinide decay chain
- Predict from simulations